

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Garg et al.

Appl. No.: 08/990,414

Filed: December 15, 1997

For:

SUPERSCALAR RISC

INSTRUCTION SCHEDULING

Art Unit: 2783

Examiner: L. Donaghue

Atty Docket: SP035.C3

Supplemental Preliminary Amendment

Assistant Commissioner for Patents Washington, DC 20231

Sir:

ant Commissioner for Patents
Ington, DC 20231

Before examination of the above-referenced patent application, Applicants submit the following amendments and remarks for consideration.

Amendments

Kindly enter the following amendments.

In the Claims

Please cancel claim 1 without prejudice or disclaimer.

Please add new claims 12-45 as follows:

12. In a computer system having a register file comprising a plurality of registers and a plurality of index-addressable temporary storage locations, a method for executing instructions having a prescribed program order, comprising the steps of:

storing a plurality of instructions in an instruction buffer, wherein each instruction (1) has an input and an output;

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